CLAIMS

What is claimed is:

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- 2 a microcode sequencer to set an identifier in a microinstruction, the identifier
- 3 indicating one of a plurality of copies of broadcast state of the processor; and
- 4 a functional unit to receive and internally store the plurality of copies of
- 5 broadcast state and to select, based on the identifier, one of the copies of broadcast
- 6 state for use in processing the microinstruction.
- 2. A processor as recited in claim 1, further comprising a memory execution unit
- 2 including a segment register, said broadcast state representing content of the
- 3 segment register.
- 1 3. A processor as recited in claim 2, further comprising a renamer to selectively
- 2 rename registers of the processor, including the segment register, wherein each of
- 3 the copies of broadcast state may correspond to a different renamed version of the
- 4 segment register.
- 4. A processor as recited in claim 1, further comprising a trace cache to maintain the
- 2 identifier for at least some of the microinstructions.
- 5. A processor as recited in claim 1, wherein the microcode sequencer comprises a
- 2 broadcast state machine to determine the identifier.

- 1 6. A processor as recited in claim 1, further comprising a second functional unit to
- 2 receive and internally store a second plurality of different copies of broadcast state
- 3 of the processor and to select, based on the identifier in a microinstruction, one of
- 4 the second plurality of copies of broadcast state for use in processing the
- 5 microinstruction.

1 7. A processor comprising:

- 2 means for generating an identifier field in a microinstruction, the identifier
- 3 field indicating one of a plurality of copies of broadcast state of the processor to be
- 4 used in processing a microinstruction; and
- 5 a functional unit including
- 6 means for receiving and internally storing the plurality of copies of
- 7 broadcast state, and
- 8 means for selecting one of the copies of broadcast state indicated by
- 9 the identifier field, and
- means for processing the microinstruction using the selected copy of
- 11 broadcast state.
- 8. A processor as recited in claim 7, further comprising a memory execution unit
- 2 including a segment register, said broadcast state representing content of the
- 3 segment register.

- 9. A processor as recited in claim 8, wherein each of the copies of broadcast state
- 2 may correspond to a different renamed version of the segment register.
- 1 10. A processor as recited in claim 7, further comprising a trace cache to maintain
- 2 the identifier field for at least some of the microinstructions.
- 1 11. A processor comprising:
- 2 a memory execution unit including a segment register, content of the
- 3 segment register representing state of the processor;
- 4 a microcode sequencer to sequence microinstructions for execution in the
- 5 processor, including setting an identifier field in at least some of the
- 6 microinstructions, the identifier field of each such microinstruction indicating one
- 7 of a plurality of copies of broadcast state of the processor to be used in processing
- 8 the microinstruction; and
- a functional unit to receive and internally store the plurality of copies of
- 10 broadcast state and to select, based on the identifier field of a microinstruction, one
- of the copies for use in processing the microinstruction.
- 1 12. A processor as recited in claim 11, further comprising a renamer to selectively
- 2 rename registers of the processor, including the segment register, wherein each of
- 3 the copies of broadcast state may correspond to a different renamed version of the
- 4 segment register.

- 1 13. A processor as recited in claim 11, further comprising a trace cache to maintain
- 2 the identifier field for at least some of the microinstructions.
- 1 14. A processor as recited in claim 11, wherein the microcode sequencer comprises
- 2 a broadcast state machine to determine the identifier field.
- 1 15. A processor as recited in claim 11, further comprising a second functional unit
- 2 to receive and internally store a second plurality of different copies of broadcast
- 3 state of the processor and to select, based on the identifier field of a
- 4 microinstruction, one of the second plurality of copies for use in processing the
- 5 microinstruction.
- 1 16. A microprocessor comprising:
- 2 a memory execution unit including a segment register file containing a
- 3 segment register, content of the segment register representing state of the
- 4 microprocessor to be broadcast within the microprocessor;
- 5 a renamer to selectively rename registers of the processor, including the
- 6 segment register;
- 7 a microcode sequencer to sequence microinstructions for execution in the
- 8 processor, including setting an identifier field in at least some of the
- 9 microinstructions, the identifier field of each such microinstruction indicating one
- of a plurality of different copies of broadcast state of the microprocessor to be used

- in processing the microinstruction, each copy of broadcast state corresponding to a
- 12 different renamed version of the segment register; and
- 13 a functional unit to receive and internally store the plurality of different
- 14 copies of broadcast state and to select, based on the identifier field of a
- 15 microinstruction, one of the copies for use in processing the microinstruction.
- 1 17. A processor as recited in claim 16, further comprising a trace cache to maintain
- 2 the identifier field for at least some of the microinstructions.
- 1 18. A processor as recited in claim 16, wherein the microcode sequencer comprises
- 2 a broadcast state machine to determine the identifier field.
- 1 19. A processor as recited in claim 16, further comprising a second functional unit
- 2 to receive and internally store a second plurality of different copies of broadcast
- 3 state of the microprocessor and to select, based on the identifier field of a
- 4 microinstruction, one of the second plurality of copies for use in processing the
- 5 microinstruction.
- 1 20. A method comprising:
- 2 storing a plurality of copies of broadcast state of a processor in each of a
- 3 plurality of functional units of the processor;
- 4 issuing a microinstruction in the processor, the microinstruction including an
- 5 identifier; and

- 6 using the identifier in at least one of the functional units to select one of the
- 7 plurality of copies of broadcast state for use in processing the microinstruction.
- 1 21. A method as recited in claim 20, wherein said broadcast state represents content
- 2 of a segment register of the processor.
- 1 22. A method as recited in claim 21, wherein each of the copies of broadcast state
- 2 may correspond to a different renamed version of the segment register.
- 1 23. A method as recited in claim 20, further comprising using a microcode
- 2 sequencer of the processor to provide the identifier.
- 1 24. A method as recited in claim 20, further comprising using a trace cache of the
- 2 processor to provide the identifier.
- 1 25. A method comprising:
- 2 providing an identifier field in a microinstruction for execution in a
- 3 processor, the identifier field indicating one of a plurality of copies of broadcast
- 4 state of the processor to be used in processing the microinstruction;
- 5 storing the plurality of copies of broadcast state in a functional unit of the
- 6 processor, and
- 7 selecting one of the copies of broadcast state in the functional unit, for use in
- 8 processing the microinstruction, according to the identifier field of the
- 9 microinstruction.

- 1 26. A method as recited in claim 25, further comprising storing a plurality of copies
- 2 of broadcast state in each of a plurality of functional units of the processor.
- 1 27. A method as recited in claim 25, wherein said broadcast state represents content
- 2 of a segment register of the processor.
- 1 28. A method as recited in claim 27, wherein each of the copies of broadcast state
- 2 may correspond to a different renamed version of the segment register.
- 1 29. A method as recited in claim 25, further comprising using a microcode
- 2 sequencer of the processor to provide the identifier field.
- 1 30. A method as recited in claim 25, further comprising using a trace cache of the
- 2 processor to provide the identifier field.